High Performance Embedded Host NVMe

Easy NVMe HOST

Host NVM Express

Key Features

- NVM Express Compliant
- Automatic PCIe/NVMe init
- IO read/write and shutdown commands
- RAM or AXI4 or Avalon interface
- 128 or 256 bits data path
- Options:
  - OPAL 2.0 management
  - Support of Pcie switch up to 8 downstream ports.
  - NVMe multi-queue management

Benefits

- Ultra low latency
- Very high throughput
- Low power architecture
- Low gate count
- No need of CPU
- Easy integration
- Ease of use

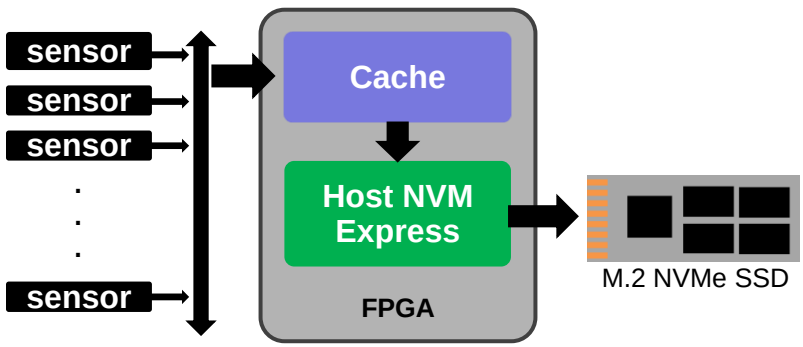
Deliverables

- Verilog RTL source code
- Low level firmware
- Synthesis scripts
- Technical documentation
- Technical support

Overview

The IPM Host NVMe is a verilog IP to be integrated in a FPGA. It fully manages the NVMe protocol on the host side without requiring any CPU. It can be used with any NVMe SSD available on the market, or with a custom design based on the NVMe Device IP from IP-Maker.

The Host NVMe is well suited for embedded applications requiring a high throughput storage such as recorder and video applications. 1+ million IOPS performance requires the use of an expensive CPU, which is not feasible in an embedded system due to cost, space and power limitation.



Using the pre-validated NVMe Host IP core greatly reduces time-to-market for storage OEM; this allows the OEM to benefit from a powerful data transfer manager. The IP-Maker Host NVMe IP core is full featured and easy to use in FPGA designs.

IP-Maker is an active contributor to the NVMe specification and also provides the NVMe device controller for data storage applications, such as NVMe SSD and NVMe NVRAM.

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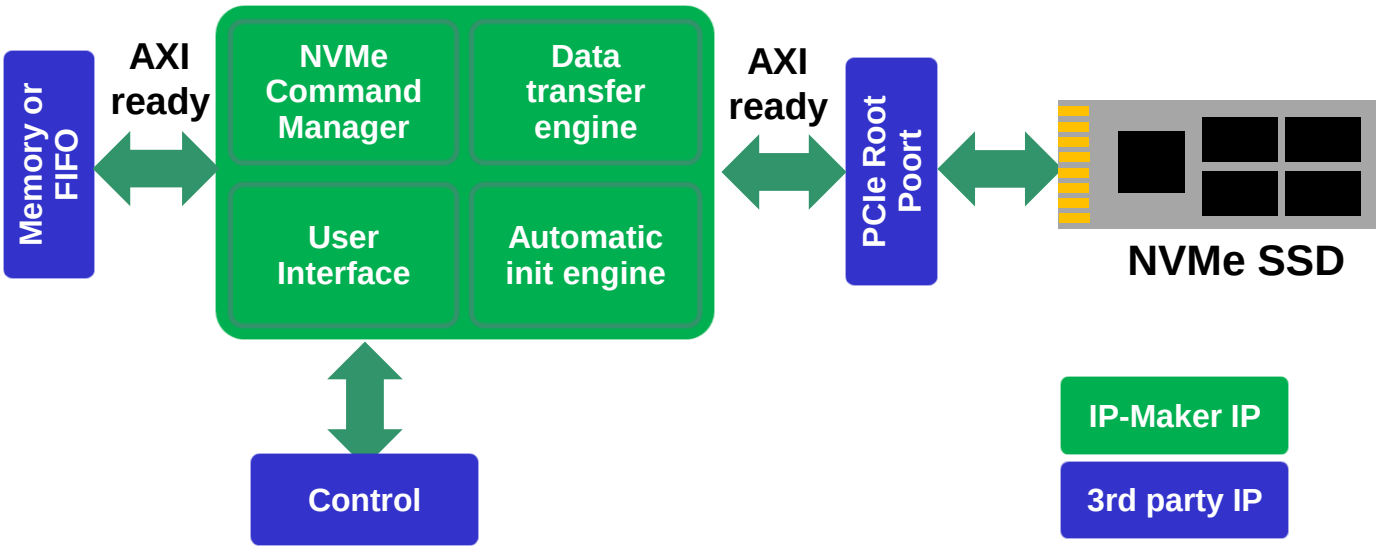
Description



The architecture of the Host NVM Express IP is based on 4 main blocks:

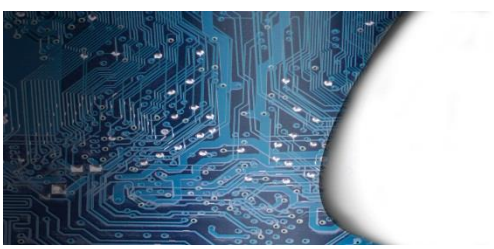
- Automatic init engine: PCIe and NVMe device initialization, hardware discovering
- User Interface: memory configuration and input for the transfer request by the API
- NVMe command manager: translation of the data request from API into a NVMe command. Submission and completion pointers management
- Data Transfer Engine: management of the data transfer between the NVMe SSD and the FIFO/memory

It delivers very low latency since it is a full hardware host NVMe implementation. That takes only few dozens of clock cycles (compared to multiple thousands of clock cycles for a software NVMe driver on a CPU). In addition, there is no needs of PCIe interrupt management because it is directly processed by the Host NVMe manager, therefore avoiding context switches.

Reference design

The NVMe Host IP is available for evaluation and demo using a reference design based on a Xilinx Ultrascale FPGA board attached to a Samsung M.2 NVMe SSD. It embeds a testbench allowing to configure the IO access : IO size, random/sequential, read/write…

Performance results: it reaches up to 3,4GB/s, which is the limitation of the SSD used (Gen3x4 NVMe SSD specification max = 3,4GB/s).



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